7, 9, 10, 17-24, 26, 27, and 30-55 under 35 U.S.C. 103(a) as unpatentable over ***Yamazaki*** (U.S. Patent No. 5,453,858) in view of ***Sawatsubashi*** (U.S. Patent No. 5,148,301) and ***Yamamoto et al.*** (U.S. Patent No. 5,426,526). Applicant respectfully traverses these rejections for the reasons set forth hereinbelow.

Applicants respectfully contend that the ***Takemura '092*** patent fails to expressly disclose or implicitly teach each and every feature necessary to anticipate or render the claimed invention obvious. For instance, in the Office Action, the Examiner contends that ***Takemura '092*** discloses a semiconductor integrated circuit chip connected to the driving circuit (Fig. 7). It should be noted, however, that Fig. 7 is a block diagram showing a thin film semiconductor integrated circuit (Col. 5, lines 7-8), and thus, ***Takemura '092*** fails to teach a semiconductor integrated circuit chip. Further, the Office Action fails to address each and every claim limitation, such as the feature concerning "at least one lightly doped drain", as set for in claims 7 and 51 of the present invention. ①

Regarding the 103 rejection based on ***Yamazaki '858***, the Examiner contends that ***Yamazaki '858*** discloses an IC (4) mounted on a substrate for controlling a driver circuit and connected to the driver circuit by COG (chip on glass). The Examiner further contends that it would have been obvious to one of ordinary skill in the art to modify ***Yamazaki '858*** by providing a memory chip or CPU chip as the IC chip as disclosed in ***Yamamoto '526***. It should be noted, however, that the reference numeral 115 of ***Sawatsubashi '301*** is merely a terminal (Col. 5, lines 13 and 34), and thus, ***Sawatsubashi '301*** fails to disclose providing an IC chip. ②

Moreover, ***Yamamoto '526*** teaches away from the use of TFTs and COG as described from (Col. 1, line 64 to col. 3, line 24; col. 14, line 67 to col. 15, line 7). Instead, ***Yamamoto '526*** prefers to use a single crystal silicon substrate as described from column 15, line 7 to column 15, line 25. Hence, it respectfully submitted that there is a lack of motivation to combine ***Yamazaki '858*** and ***Yamamoto '526*** because ***Yamamoto '526*** teaches away from using TFTs and COG.

The Examiner further contends that it would have been obvious to use a bottom gate type TFT in the active matrix and a top gate type TFT in the driving circuit as set

forth in claim 36. However, in reviewing the prior art of record, Applicant contends that this basis for rejection is improper because this feature is not expressly disclosed or inherently described in any of the prior art of record. Further, the Office Action fails to address each and every claim limitation, such as the feature concerning "at least one lightly doped drain", as set for in claims 7 and 51 of the present invention. Accordingly, Applicant requests in the next communication that evidence be provided showing these claimed features or withdrawal of the rejection.

With respect to Double Patenting rejection, Applicant respectfully request that this rejection be held in abeyance until the aforementioned prior art rejections have been overcome.

In view of the foregoing, Applicants respectfully submit that the application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited. Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285
Nixon Peabody LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

EJR/TAV:jes